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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,875	06/11/2001	Abu K. Eghan	X-901 US	4969

24309 7590 01/30/2002

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER

BHAGAWAN, VENKATESHA S

ART UNIT	PAPER NUMBER
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2829

DATE MAILED: 01/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/879,875

Applicant(s)

EGHAN ET AL.

Examiner

Vinny S Bhagawan

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 June 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

Detail action

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes,"

1) Specifically, the Abstract is objected because it contains phrases and words such as "present invention", "improved", "The invention discloses". Correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2) Claims 1-3, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al., U.S. Patent Number 5,739,585 in view of Lim et al., U.S. Patent Number 6,020,221.

In regards to claims 1 and 2 , Akram et al. disclose (col. 4, lines 4-30 and FIG. 1) a packaged integrated device consisting of a substrate having a recessed central region, surrounded by a raised perimeter, the central region and the perimeter being formed together from the same material. The central region also has a die mounting location in which an integrated circuit device can be flipped and mounted face down.

While Akram et al. fail to teach how the integrated device is electrically connected to the substrate, Lim et al. illustrate (FIG.8) a semiconductor substrate having a plurality of contacts in the central region in which an integrated circuit device formed with contacts on a top surface, flipped and placed against the central region of the substrate making contact with the contacts of the central region of the substrate. Lim et al. also teach (col. 3, lines 36-52; col. 5, lines 32-42) a method of connecting an integrated circuit device to a substrate in which the method includes electrically connecting the contacts of the central region of the substrate to solder balls on an external surface of the packaged integrated circuit device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to package an integrated circuit device on a substrate as disclosed by Akram et al. and connect it electrically to the substrate as disclosed by Lim et al., since such a package reduces the warpage

and stresses caused during the assembly process and further increases the reliability and yield of the packaged devices.

3) In regards to claim 3, Lim et al. state (col. 5, lines 55-57) that the most commonly used material for the substrate is ceramic since any material used for the substrate must be able to withstand high temperatures.

4) In regards to claim 5, while Lim et al. fail to mention a specific type of contact in the central region of the substrate, FIG. 8 clearly illustrates that the contacts in the central region could be solder bumps.

5) Claims 4, and 6-8 are rejected under U.S.C. 103 (a) as being unpatentable over Akram et al. in view of Lim et al. as applied to claims 1-3 and 5 above, and further in view of Hoang, U.S. Patent Number 6,201,301 B1.

In regards to claim 4, Hoang discloses a flip chip package in which the substrate used could be fabricated from a material comprising a glass-ceramic material (col. 1, lines 64-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a ceramic material that also includes glass for the substrate, since it is well known that such a material is a good substitute for ceramic.

6) Concerning claims 6-8, Hoang also describes (col. 2, lines 32-40, and FIG. 1) the flip-chip package to include a heat spreader connected to an integrated circuit device

with thermal grease and contacting a stiffener that is essentially a raised perimeter of the substrate. But, Hoang fails to teach that the integrated circuit device and the heat spreader are recessed such that the upper surface of the heat spreader is planar with an upper surface of the raised perimeter. However, one of ordinary skill in the art at the time the invention was made would be motivated to keep the integrated circuit device and the heat spreader recessed such that an upper surface of the heat spreader is planar with an upper surface of the raised perimeter as this would reduce the package thickness and results in a more compact overall package.

7) Claims 9 is rejected under U.S.C. 103 (a) as being unpatentable over Akram et al. in view of Lim et al. as applied to claims 1-3 and 5 above and further in view of Malladi, U.S. Patent Number 5,939,782.

While Akram et al. and Lim et al. fail to teach the inclusion of a capacitor for the packaged integrated circuit, Malladi teaches (col. 1, lines 41-63, col. 2, lines 18-60) incorporation of one or more capacitors in a variety of locations in semiconductor packages including a flip-chip package, for reduction of power transients, and how these capacitors are electrically connected to the power and ground contacts of the integrated circuit device. Therefore it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate a capacitor in the packaged integrated circuit device. One would be motivated to do so to reduce power transients and to improve voltage stability. Further, although Malladi does not specifically mention a raised perimeter/peripheral area for the location of one or more capacitors, however

one of ordinary skill in the art at the time the invention was made would be motivated to extend the function of a raised perimeter/peripheral area to include an auxiliary device such as a capacitor so as to achieve a more compact package.

8) Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al., U.S. Patent Number 5,739,585 in view of Lim et al., U.S. Patent Number 6,020,221 and further in view of Malladi, U. S. Patent Number 5,939,782.

Referring to claims 10 and 11, Akram et al. disclose (col. 4, lines 4-30 and FIG. 1) an integrated circuit package consisting of a substrate having a recessed central region, and a raised peripheral area. Although Akram et al. do not disclose a plurality of contacts in the central region, however Lim et al. illustrate (FIG.8) a semiconductor substrate having a plurality of contacts in the central region for providing electrical contact to an integrated circuit device. While Akram et al. and Lim et al. fail to teach the inclusion of a capacitor for the packaged integrated circuit, Malladi teaches (col. 1, lines 41-63, col. 2, lines 18-60) incorporation of one or more capacitors in a variety of locations in semi conductor packages including a flip-chip package, for reduction of power transients, and how these capacitors are electrically connected to the power and ground contacts of the integrated circuit device. Therefore it is obvious to one of ordinary skill in the art at the time the invention was made to incorporate a capacitor in the packaged integrated circuit device. One would be motivated to do so to reduce power transients and to improve voltage stability. Further, although Malladi does not specifically mention a raised perimeter/peripheral area for the location of one or more

capacitors, however one of ordinary skill in the art at the time the invention was made would be motivated to extend the function of a raised perimeter/peripheral area to include an auxiliary device such as a capacitor so as to achieve a more compact package.

9) In regards to claim 12, the examiner takes official notice that it is well known that the ground and power terminals of an integrated circuit package substrate can be respectively connected to the ground and power supply terminals of the integrated circuit device.

Therefore it is obvious to one of ordinary skill in the art at the time the invention was made to derive the ground and power voltages required for the operation of the integrated circuit device by connecting the ground and power terminals of the packaged substrate to the respective terminals of the integrated circuit device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vinny S Bhagawan whose telephone number is 703-305-2717. The examiner can normally be reached on 7:30AM to 4:00PM, Monday through Thursday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 703-308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-4084 for regular communications and 703-308-4084 for After Final communications.

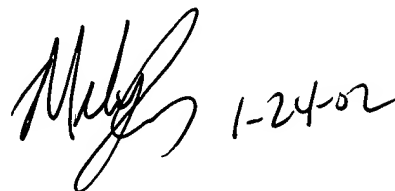
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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-5486.

January 23, 2002

A handwritten signature in cursive script, followed by the date "1-24-02".

MICHAEL J. SHERRY
PRIMARY EXAMINER